LAN AND WAN TIMING CONSIDERATIONS FOR PMC-SIERRA ATM PHY DEVICES

Preliminary Information

Issue 1: September, 1996

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OVERVIEW

PMC-Sierra's ATM Physical Layer products comply to the North American Synchronous Optical Network (SONET) and the European Synchronous Digital Hierarchy (SDH) framing formats. Local Area Network (LAN) systems designed with these devices can easily be interfaced to SONET/SDH-based Wide Area Network (WAN) equipment without the need for data format conversion; more traditional LAN technologies, such as Ethernet, require some form of format conversion or encapsulation in order to be carried over the WAN. However, even with compatible data formats, the LAN equipment at this interface needs to satisfy certain WAN timing requirements. LAN equipment may be connected to the WAN via a "gateway" or by making the LAN network elements part of the WAN. In either case, the gateway or the LAN element is now part of the WAN, and this Network Element (NE) now has to deal with specific WAN timing issues such as jitter accumulation and wander (low frequency jitter).

Timing requirements for the LAN are usually not an issue. Local area networks connect points physically close together, typically less than 100 meters to no more than 1-2 km. Because of their proximity, these connections are usually implemented with few or no repeaters. Also, there is typically one source of timing that is used to time all nodes. As a result, jitter accumulation and timing issues due to wander do not exist.

Metropolitan Area Networks (MAN) typically cover larger distances, up to 100 km. These networks can have a large number of repeaters, so jitter accumulation can pose a problem. In this case, WAN jitter-related specifications for NE should be observed. However, the distances covered are not large enough to cause significant wander-related problems.

Wide Area Networks cover even larger distances and consist of large numbers of NE and repeaters. Jitter accumulation in these networks is significant and the NE should satisfy jitter-related requirements for the particular type of WAN. Synchronous WAN (i.e., SONET based) will also experience problems related to wander, therefore, the NE should satisfy the wander-related requirements for SONET NE. To meet the wander specification, the transmit clock synthesis must utilize a narrow Phase Locked Loop (PLL) bandwidth.

Most of this application note deals with addressing the North American SONET timing requirements. The European SDH requirements are somewhat different due to SDH not using the traditional North American hierarchical timing distribution scheme.

BACKGROUND AND DEFINITIONS

Network Synchronization

In the past, a method of synchronizing the North American digital network was specified to handle the timing requirements of digital communications. These requirements were defined in Bellcore GR-436-CORE Digital Network Synchronization Plan. This plan defined a hierarchical network based on stratified clocks. At the top of the network hierarchy there are the Stratum 1, or Primary Reference Source (PRS), clocks that are used to reference Stratum 2 clocks. These Stratum 2 clocks, in turn, reference Stratum 3 clocks. This is illustrated in figure 1.

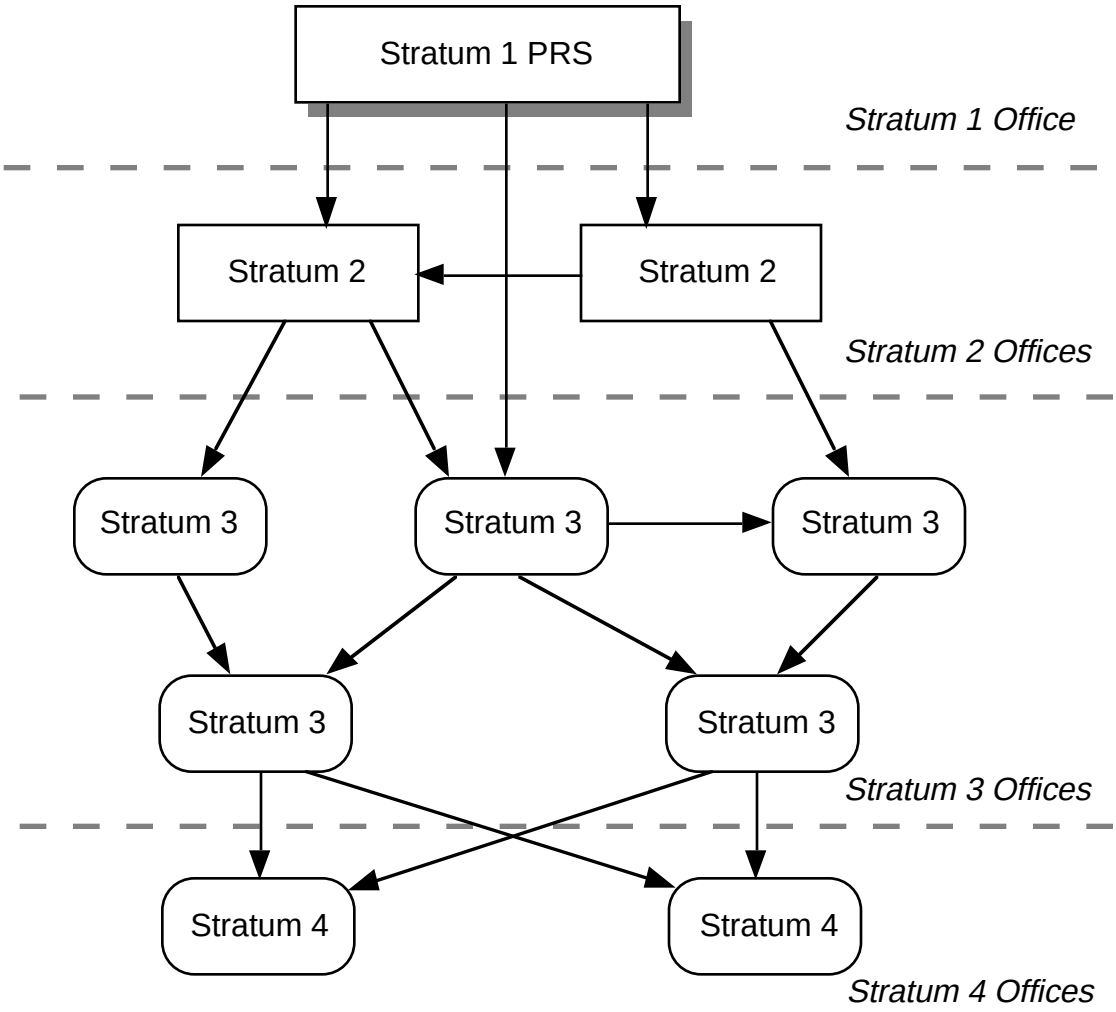


Figure 1: Timing Hierarchy

The quality of these clocks is shown in table 1. The hierarchy dictates that equipment be timed by either a higher layer stratum clock (lower stratum number) or a peer layer

clock that itself is timed to a higher stratum layer. A new stratum clock is being defined; the SONET Minimum Clock (SMC).

Stratum Level	Free-Run Accuracy (ppm)	Holdover Stability (ppm)	Pull-in/ Hold-in (min ppm) [1]	Typical Clock Source
1	$\pm 10^{-5}$	N/A	N/A	Cesium beam atomic clock
2	$\pm 1.6 \times 10^{-2}$	$\pm 1 \times 10^{-4}$ per day	capable of sync'ing to clock with accuracy of $\pm 1.6 \times 10^{-2}$	Double Oven VCXO or Rubidium atomic oscillators, digital long time constants
3E	± 4.6	$\pm 1 \times 10^{-2}$	capable of sync'ing to clock with accuracy of ± 4.6	Ovenized or TC VCXO with better stability in holdover than stratum 3
3	± 4.6	<255 slips during first day of holdover	capable of sync'ing to clock accuracy of ± 4.6	Ovenized or TC VCXO
SMC	± 20	no holdover	capable of sync'ing to clock accuracy of ± 20	VCXO
4E	± 32	no holdover	capable of sync'ing to clock accuracy of ± 32	VCXO
4	± 32	no holdover	capable of sync'ing to clock accuracy of ± 32	VCXO

Table 1: Stratum Timing

Stratum Level	Filtering of Clock	Transient Response
1	N/A	N/A
2	Yes (f_c= 0.01Hz)	MTIE ≤ 150ns (see Fig 10)
3E	Yes (f_c= 0.01Hz)	MTIE ≤ 150ns (see Fig 10)
3	No (f_c= 3Hz)	MTIE ≤ 150ns and Phase Change slope ≤81ns in any 1.326ms interval
SMC	MTIE, TDEV per GR-253 (f_c= 0.1Hz)	MTIE ≤ 1µs (see Fig 10)
4E	No	MTIE ≤ 1µs and Phase Change slope ≤81ns in any 1.326ms interval
4	No	No requirement

Table 1: Stratum Timing - cont'd

[1] The clock requires 2x the min ppm pull-in range in order to achieve lock since it may be running at one end of its accuracy range and the reference it is locking to is running at the other end of its range.

Timing Distribution

Digital network synchronization in North America is based on the Building Integrated Timing Supply (BITS) clock. The BITS unit clock is the master timing supply for an entire building. It is the most accurate and stable clock in the building (i.e. the lowest stratum number clock in the building). The stratified clock in the BITS unit is locked to an "upstream" timing reference such as a PRS, or one of a number of recovered clocks from the incoming digital services. The BITS unit outputs a number of DS-1 framed all-ones signals that are distributed through the building to various equipment. The timing is independent of type of service provided by the equipment. For redundancy, usually two BITS clocks are delivered to time the equipment in the unlikely event that there is a connection failure within the building.

The GR-436-CORE specification requires that the facility data link in the Extended Super Frame (ESF) format be used to carry a *Synchronization Message*, identifying the source of the timing used by the equipment. Equipment that uses a BITS clock as its timing reference is defined to be *externally timed*.

Evolution of the Network Synchronization Plan

SONET provides a high quality, low bit error rate network. Transport overhead bytes allow Bit Interleaved Parity (BIP) errors and Far End Block Errors[2] (FEBE) to be monitored to check the integrity and quality of the transmission. In addition, the deployment of SONET created the need for new nodes, many of which did not have access to BITS clocks. As a result, the SONET optical signal (OC-N) began being used to carry timing synchronization.

This prompted a need to merge the classic digital network synchronization with the new SONET-based one. In the future, the digital network synchronization will likely be entirely SONET-based, but at present it is a hybrid between the two concepts. It is recommended that, when available, the OC-N signal be used to generate a DS-1 framed all-ones signal as a reference for the BITS unit to, in turn, derive an output DS-1 framed all-ones signal timing source. In addition, a few "rules" are defined for the NE to ensure the compatibility of network synchronization using BITS clocks and SONET-based synchronization:

1) Where BITS timing is available, SONET NE (Network Elements) clocks are *externally* timed to the BITS clock;
2) External-timing references to a SONET NE are from a BITS clock of stratum 3 or better quality.
3) Where no BITS timing is available, SONET NE clocks are timed from a received OC-N signal;
4) Timing signals delivered to the synchronization network from a SONET NE are derived directly from a terminating OC-N, not a VT1.5 mapped signal.

[2] An indication of BIP errors occurring at the remote receiver.

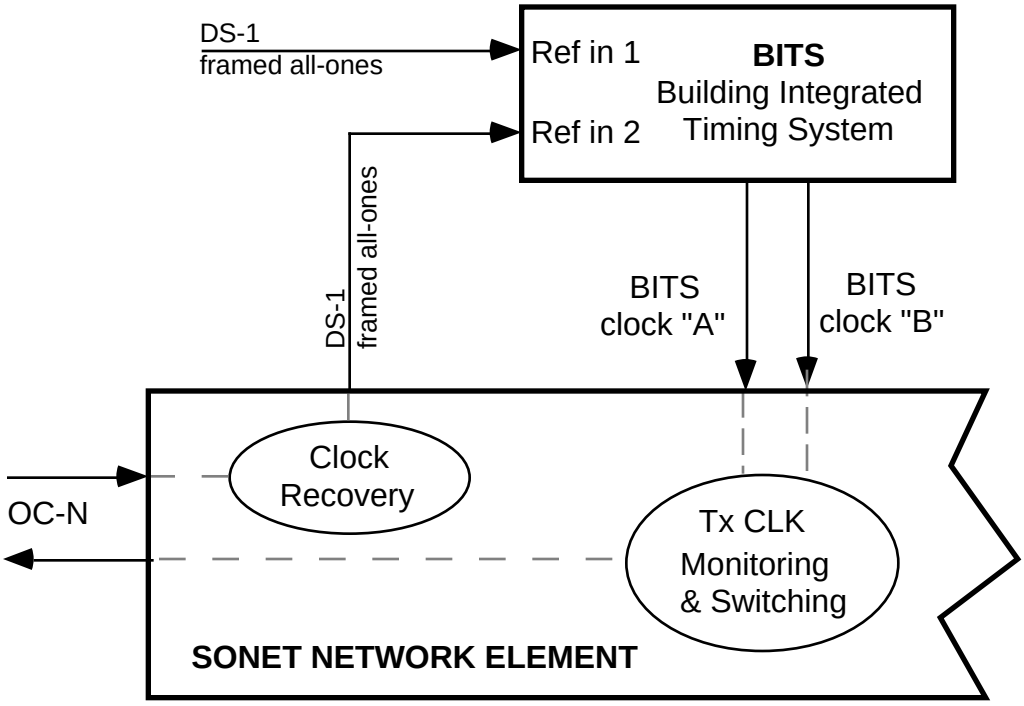


Figure 2: BITS Timing Reference derived from incoming OC-N

Synchronization Messaging

As mentioned previously, the GR-436-CORE specification requires that a *Synchronization Message*, identifying the source of the timing used by the equipment be carried in the ESF facility datalink. SONET has a similar way to carry the synchronization status message, using the lower order nibble (bits 5-8) of the S1 (Z1) byte in the line overhead.

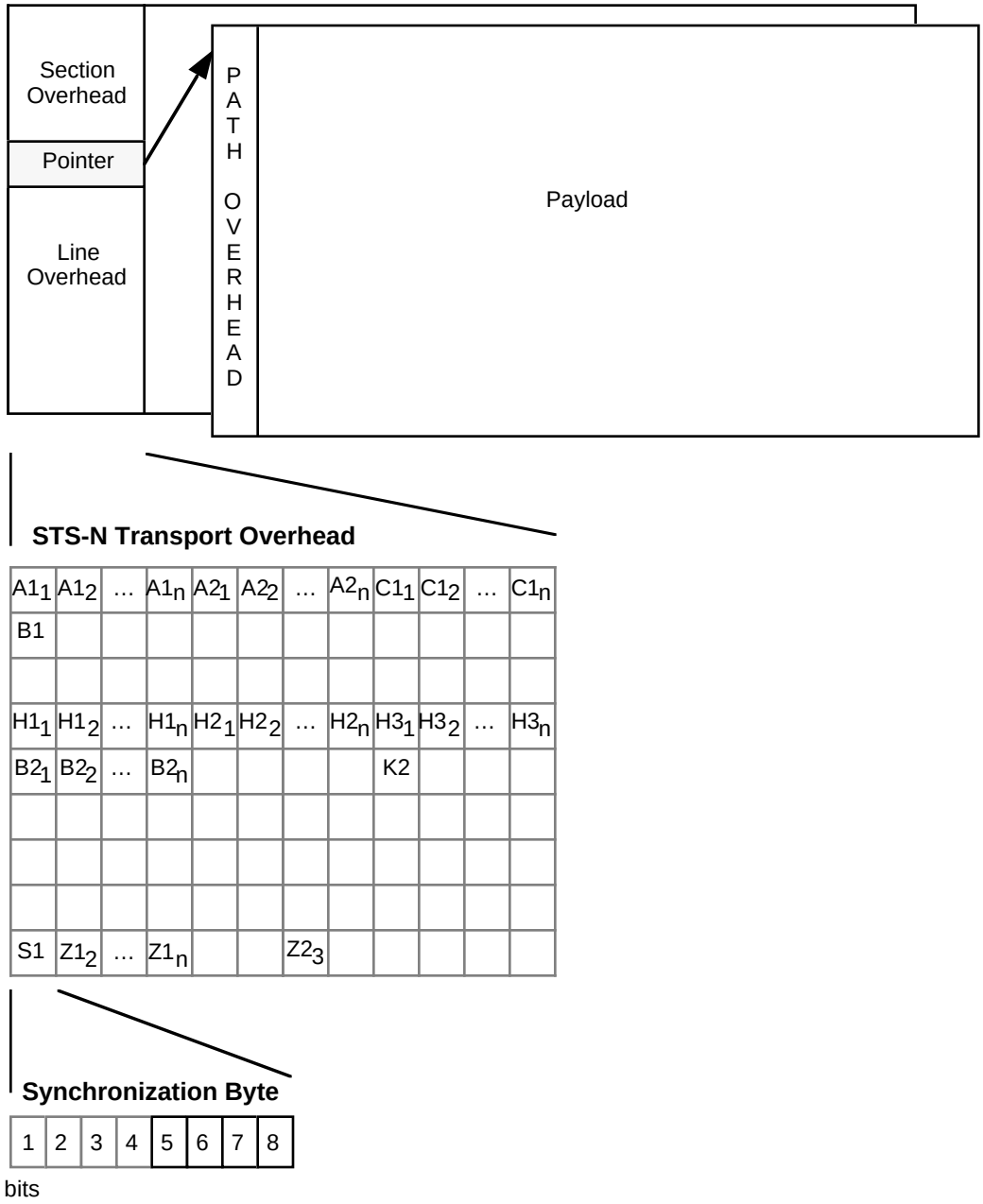


Figure 3: Synchronization Status Byte Location

Synchronization status messages convey clock quality information that allows the SONET network element to select the most suitable synchronization reference from the set of available references. Unlike plesiochronous digital networks that relied on the defined timing hierarchy topology, SONET topology allows for rings which can result in the creation of timing loops.

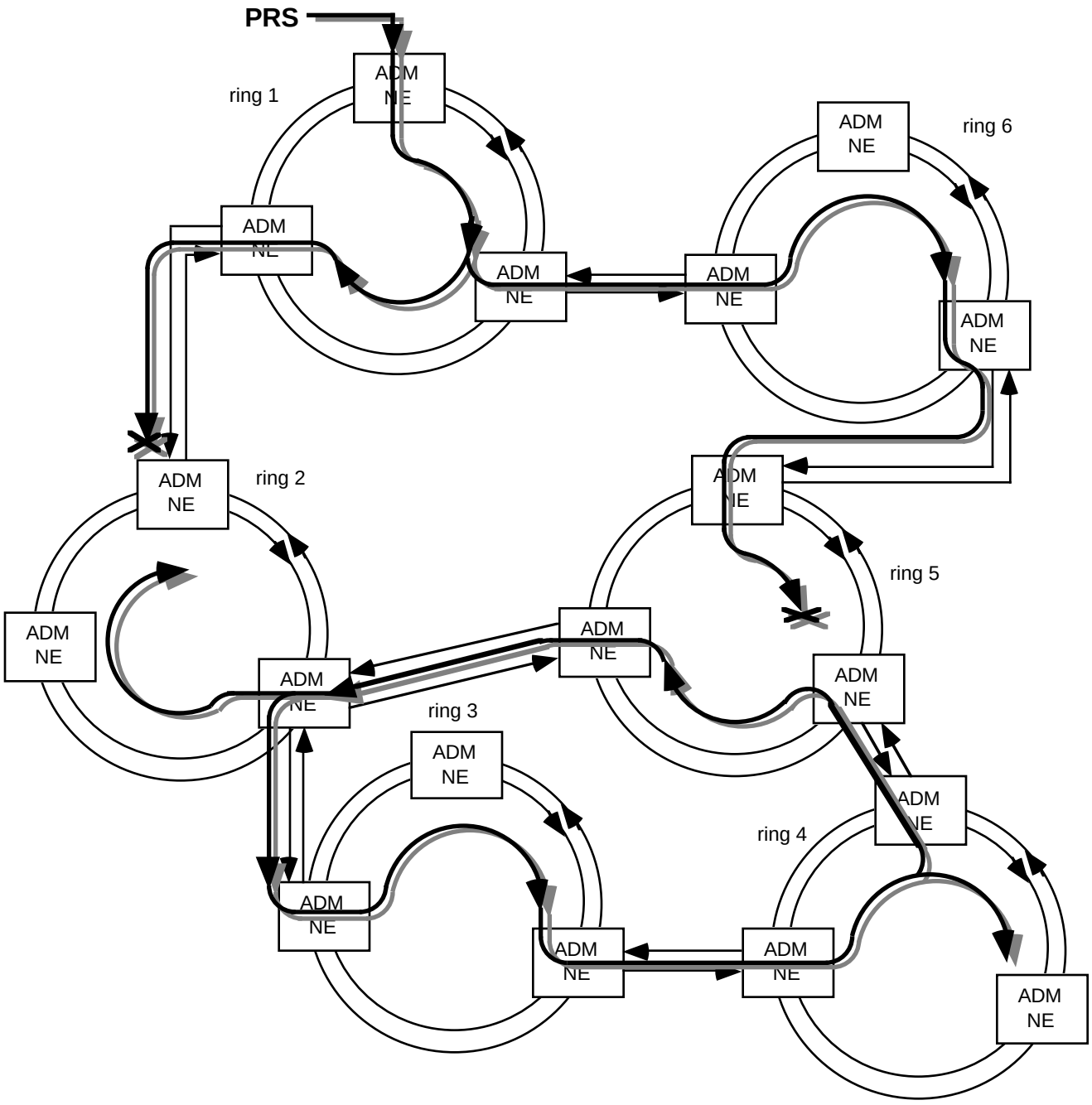


Figure 4: Generation of Timing Loops in SONET Rings

Figure 4 illustrates a potential occurrence of a timing loop. In this example, the head-end (top node, ring 1) is externally timed with a PRS and all other nodes are line timed. Ideally, the nodes interconnecting adjacent rings should all derive their timing from a line such that every node in every ring is ultimately timed back to the PRS (i.e., the bottom-right node of ring 5 derives its timing from the top node of ring 5, and the

timing path from ring 4 to ring 5 does not exist). A possibility exists, through mis-configuration or through an automatic switch of reference timing to an alternate source in the event of signal degradation, that a timing loop is created. Here, a timing loop arises when the bottom-right node of ring 5 changes the source of its derived timing from the active "inner fiber ring" to the line from the top-node of ring 4. The clock frequency in this loop will very slowly change depending on the stability of the oscillators in the node and any perturbations introduced in the loop.

The Synchronization Status Messages (shown in Table 2) were defined to help avoid creating this timing loop by "tagging" each line with an indication of the quality of its timing source. The intent is that each NE choose the better quality level clock to time itself to. However, in a ring topology, the potential to create a loop still exists even with these status messages. Again, using figure 4 as an example, each node will see each incoming line tagged with the "PRS" status message, indicating that the timing traces back to an externally applied Stratum 1 source. Therefore, any node can decide to reference itself to any number of potential timing sources, including ones that would result in the creation of a loop. In an effort to resolve this timing loop problem, work is continuing in the standards bodies to extend the status message definition to include a "hop" count that indicates how far away from the PRS a node's timing reference is located. This "hop" count, possibly carried in the upper nibble of S1, would be used to select the appropriate reference; the lower the hop count, the "better" the quality of timing reference. Until this extension is approved, careful synchronization planning is necessary to avoid timing loops even if the status messages are used.

Description	Acronym	Quality level	DS-1 FDL Code Word	S1 (bits 5-8)
Stratum 1 Traceable	PRS	1	0000010011111111	0001
Synchronized-Traceability Unknown	STU	2	0000100011111111	0000
Stratum 2 Traceable	ST2	3	0000110011111111	0111
Stratum 3 Traceable	ST3	4	0001000011111111	1010
SONET Minimum Clock Traceable	SMC	5	0010001011111111	1100
Stratum 4 Traceable	ST4	6	0010100011111111	N/A
Don't Use for Synchronization	DUS	7	0011000011111111	1111
Reserved for Network Synchronization Use	RES	—	0100000011111111	1110

Table 2: Synchronization Status Messages

An additional problem with timing can arise due to the use of status messages. Older NE that do not support the Synchronization Status Message in S1 byte will transmit the default all-zeros SONET overhead byte in the S1 position, resulting in an all-zero status nibble corresponding to the "Synchronized-Traceability Unknown" code. This

status message indicates that the timing for this OC-N is synchronized and has a very good quality clock (low Quality Level number), second only to the PRS. A NE receiving this OC-N and this status message would conclude that this timing should be used. However, the older NE originating this “false” message may not be synchronized to any reference and, in fact be free-running with a ± 20 ppm oscillator. Again careful synchronization planning is required to avoid this pitfall.

SONET Timing Modes

SONET offers four timing modes: external, line, loop and through mode.

In *external-timing* mode, the BITS clock provides the timing to the NE. The BITS unit can itself be referenced to an OC-N signal or some other timing source.

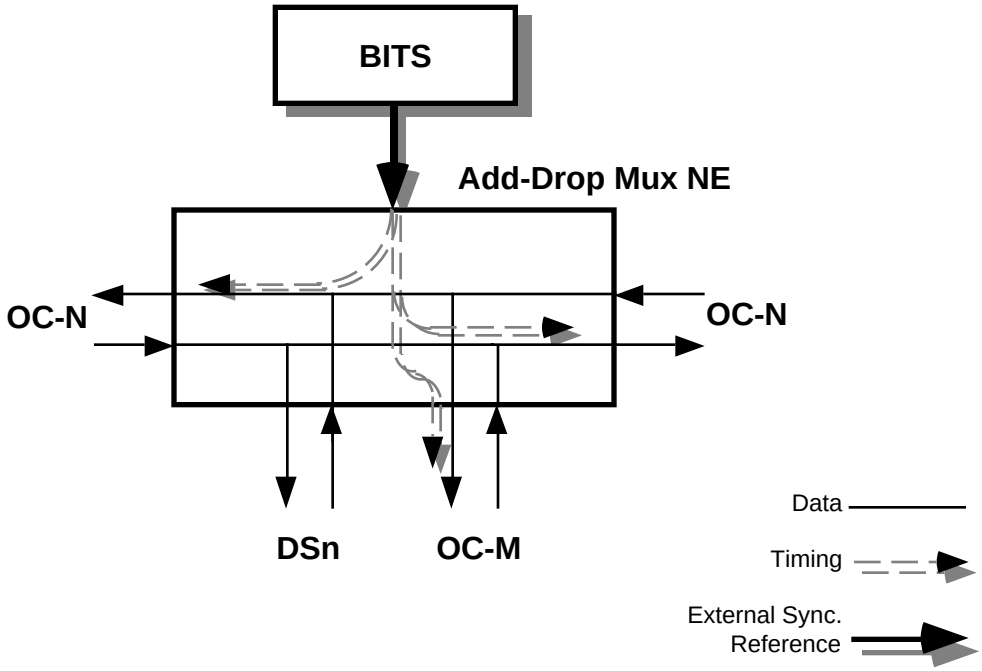


Figure 5: External Timing Mode

In *line-timing* mode, one of the received OC-N signals is used to derive timing for the entire NE.

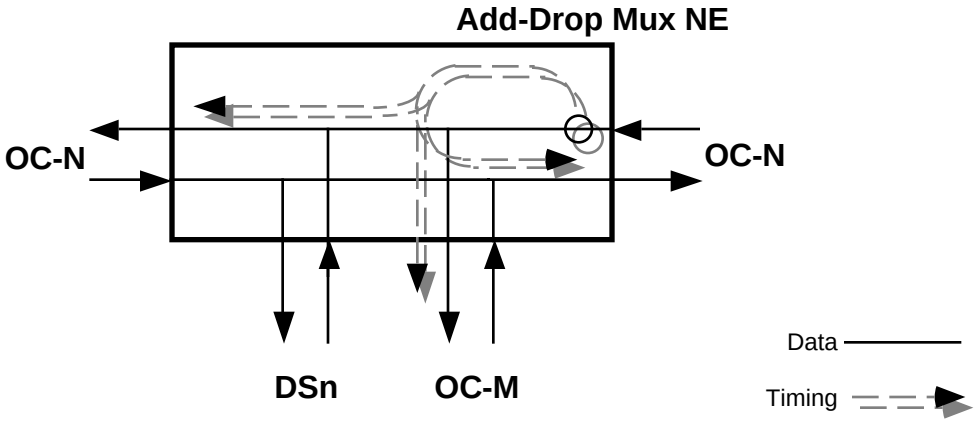
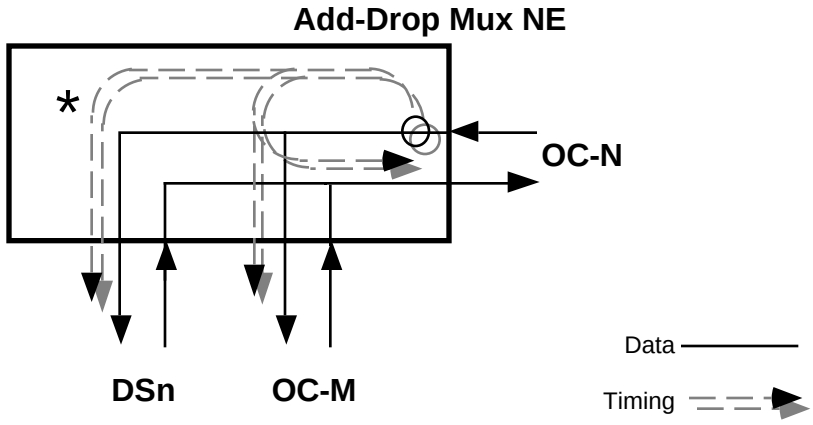


Figure 6: Line Timing Mode

The *loop-timing* mode is a special case of the line timing mode but is defined separately because it currently has no requirement for clock holdover. However, holdover may be added in the future.



***** timing used in synchronous mapped;
not used in async mapped.

Figure 7: Loop Timing Mode

The *through-timing* mode is the standard timing mode for regenerators. It is not recommended as a timing mode for NE because it creates two timing sources in the network that was supposed to be synchronous.

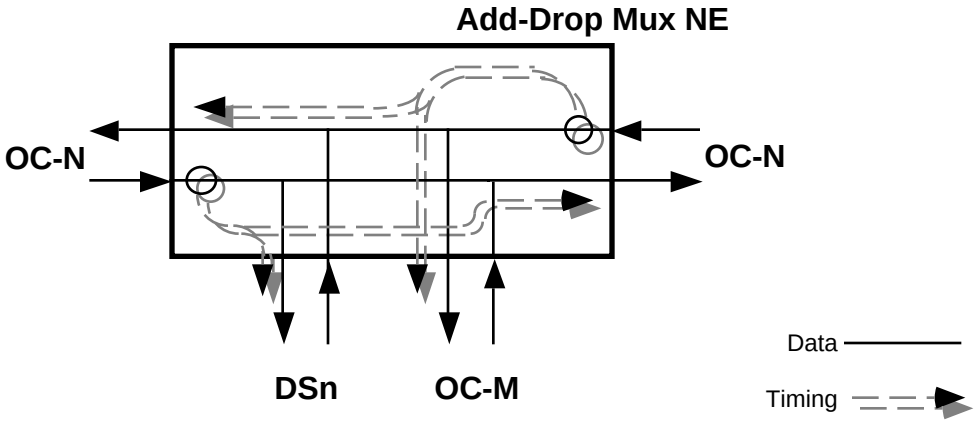


Figure 8: Through Timing Mode

WANDER in WAN Timing

Sources of Wander

Digital clocks exhibit pulse position modulation, that is, a deviation of the edges from the ideal clock edge positions . Pulse position modulation frequencies above 10 Hz are defined as jitter, while modulation frequencies below 10 Hz are defined as wander. Jitter is typically attributable to additive Gaussian noise, whereas wander is typically attributable to slowly varying environmental conditions.

The sources of low frequency modulation resulting in wander can be varied; these include changes in operating temperature and $\frac{1}{f}$ (or "flicker"[3]) noise . An oscillator locked to wander-free reference clock in a narrow bandwidth phase lock loop will exhibit wander above the frequencies where the open loop gain is below 0 dB. In digital network synchronization, a very narrow PLL (below 0.1 Hz) is used in order to filter accumulated wander from the PRS to the generated timing reference. These clocks have to satisfy short term stability requirements and limit the amount of wander they produce. In Bellcore and ANSI the clocks are stratified according to their long term stability, and limits are set for short term stability.

Changes in operating temperature cause wander due to the resulting variations in the light propagation properties of the fiber. A light pulse propagates through a long fiber

[3] Flicker noise is found in all active devices and in some passive devices. The origins of flicker noise are varied, but its characteristic is a1/f spectrum. This noise is always associated with flow of direct current.

cable with a given velocity. When the index of refraction is changed due to a temperature variation, the propagation velocity through fiber cable is also changed. Effectively, it looks like the length of the fiber cable is changing and the transmitter is moving away or toward the receiver. This is similar to a Doppler effect; at one end, the transmitted data is sent at one frequency and the data is received at other end with a different frequency. Once the temperature variation stops, the index of refraction settles down to a new value and the transmitted and received frequencies once again become the same.

The LASER output frequency also changes with temperature. Similarly, the propagation delay of the light pulses in the fiber differs with the different wavelengths. This results in a similar frequency differential effect as before.

The resultant magnitude of the wander becomes significant as the length of the fiber increases; for example, in an above-ground fiber cable 250 km long carrying an OC-3 signal, a 20 degree temperature change will result in a 26 bit difference between the transmitted and received data! Appendix A shows the derivation of the temperature effects.

Effects of Wander

The synchronous optical network has several advantages to a plesiochronous network: buffer size is minimal because the receive and transmit rate of OC-N signals are the same; and there is a minimal delay for through traffic because the rate of dropped and added traffic is the same. Although all the nodes run synchronously, practically, two NE are not always operating with exactly the same clock due to jitter and wander effects. SONET uses a concept of pointer movements to allow the Synchronous Payload Envelope (SPE) to run synchronously to the transport overhead. The line overhead bytes H1 and H2 contain a pointer value indicating a relative offset position to the start of the SPE. Pointer movements provide the ability to insert or remove an entire byte of the SPE to rate-adapt it to the transmit line rate; they should happen infrequently.

In Add-Drop Multiplex (ADM) NE, the through-traffic SPE bytes are put into a FIFO buffer together with any add-traffic bytes at that node. These bytes are read from the FIFO using the transmit clock and inserted into the outgoing SONET frame. The number of bytes written to the FIFO and the number of bytes read from the FIFO should be the same. If more bytes are written into the FIFO than are read from it, then eventually the FIFO will overflow and data will be lost. Pointer movements are performed to manage this FIFO depth and to keep it from overflowing.

The FIFO size should be small enough to minimize the delay through it but large enough to tolerate input jitter and the infrequent pointer movements. The problems associated with wander are two-fold; a pointer movement (equivalent to 8 UI of instantaneous jitter) coupled with “normal” line jitter can cause the FIFO to overflow, or a large number of frequent pointer movements alone can cause the FIFO to overflow. Typically, the overflow will happen at some receiving NE downstream after

wander and jitter have had a chance to accumulate, hence the need for wander filtering and control of wander generation.

Finally, even a simple difference in average frequency between the transmit and receive data, although small, can result in substantial phase change if it persists for a long time. This will also introduce pointer movements which, depending upon the FIFO fill levels and accumulated jitter of downstream NE, can result in a FIFO overflow. Although the SONET Minimum Clock (SMC) accuracy is ± 20 ppm , GR-253 notes that payload integrity is not guaranteed for frequency offsets larger than ±4.6 ppm. Actually, some Bellcore Client Companies (BCC) may require stratum 3 clocks for SONET NEs used in applications that do not explicitly require stratum 3 clocks (such as ATM). It is advisable to use stratum 3 clocks when interfacing LAN services to the WAN so that the free-running accuracy of the ATM traffic transmit clock will be better than 4.6 ppm and not perturb the pointer positions in downstream NE.

Excessive pointer movement culminate in desynchronizer FIFO errors. For example, corruption of the DS1 streams mapped into VT1.5 tributaries by pointer movements in the desynchronizer will cause downstream network impairments (i.e., loss of frame). In ATM payloads carried over SONET, excessive pointer movement should not present a problem. Nevertheless a SONET network is designed to carry both ATM and VT-mapped payloads; ATM services are burdened with the synchronization requirements for VT structured SPEs.

STANDARDS REQUIREMENTS

What do the Standards bodies want?

For proper operation of the WAN network, NE timing circuits:

- need to satisfy requirements for frequency accuracy, stability, pull-in and hold-in;
- they have to be configurable for various timing modes;
- they need to be designed for high reliability (i.e., redundancy);
- they need to be able to transition “gracefully” when switching from one timing reference to another;
- they need to provide filtering of wander and jitter;
- they need to have a high tolerance to incoming wander and jitter; and
- they must not generate much wander and jitter.

Clock Stratification and Reliability:

As mentioned previously, GR-1244-CORE defines different layers of clocks with various degrees of accuracy and stability. In North America, the master-slave network synchronization approach is used, which defines certain pull-in and hold-in ranges for each stratified clock. These ranges are required to ensure that a certain level clock can lock to a reference clock of the same or better stratum level. There is also a requirement for the stratum clock to reject a reference that is outside the frequency band defined by the pull-in and hold-in range (this frequency band is approximately three times the free-run accuracy range of the clock).

In a WAN NE, a timing failure can result in loss of a large amount of traffic and potential revenue. Therefore, it is important to provide redundancy for NE timing circuitry, usually in the form of two separate synchronization cards. One card acts as a timing master and supplies the clock to all NE interfaces as well as to the slave synchronization card. In the case of a master card failure, the slave card will take over and supply the clock to all interface cards. This is explained fully in section 3.3, Duplication of Equipment of General Functional Requirements, of [3]; and in section 5.4.4.3.1, Clock Hardware, of [1].

Similarly, to avoid loss of traffic, the transition of timing from one reference to another (as in the case of a redundancy switch or simply a change in timing reference) must be graceful, i.e., it should not cause phase transients above an allowed level. In addition, in the event there is no reference to switch to, holdover requirements should be met. Holdover requires that the timing circuitry maintain the last known good frequency for as long as possible once the reference is lost. Holdover frequency stability is defined for a period of 24 hours over a temperature range. This temperature range differs for different types of equipment. For normal central office equipment, ±5 °F variation over a day is considered reasonable. Previous versions of the SONET specifications required a holdover stability of ±4.6 ppm in 24 hours and over ±32 °F; the applicable temperature range depends on the actual operating environment.

Wander:

WAN equipment has to satisfy certain requirements regarding wander and jitter. Jitter is a familiar term, used to describe "… the short-term variations of a digital signal's significant instants (e.g., optimum sampling instants) from their ideal positions in time." [3] Wander is defined "… as the long-term variations of the significant instants (e.g., zero level crossings) of a digital signal from their ideal positions in time." [3] The distinction comes down to frequency: jitter is defined at frequencies of 10 Hz and above, while wander is defined at frequencies below 10 Hz . As a result, there is a distinction in the way the limits are specified. Jitter is specified in terms of UI (unit Interval) RMS or Peak-to-Peak, but sometimes it can be specified in units of time (e.g. nanoseconds) or phase (e.g. degrees); wander is specified in terms of Maximum Time Interval Error (MTIE) and Time Deviation (TDEV).

The MTIE is used to describe the frequency offset of a clock from its ideal frequency, and the phase changes of the clock, over an "observation" period. MTIE is in units of nanoseconds of peak-to-peak wander.

The TDEV is used to describe the spectral content of the clock. Its units are RMS nanoseconds of wander.

In order to determine the MTIE and TDEV parameters of a clock, the Time Interval Error (TIE) must be measured. TIE is the time difference between a perfect clock and the observed clock (in figure 9, below, it is $\Delta\tau 1$, $\Delta\tau 2$, ...).

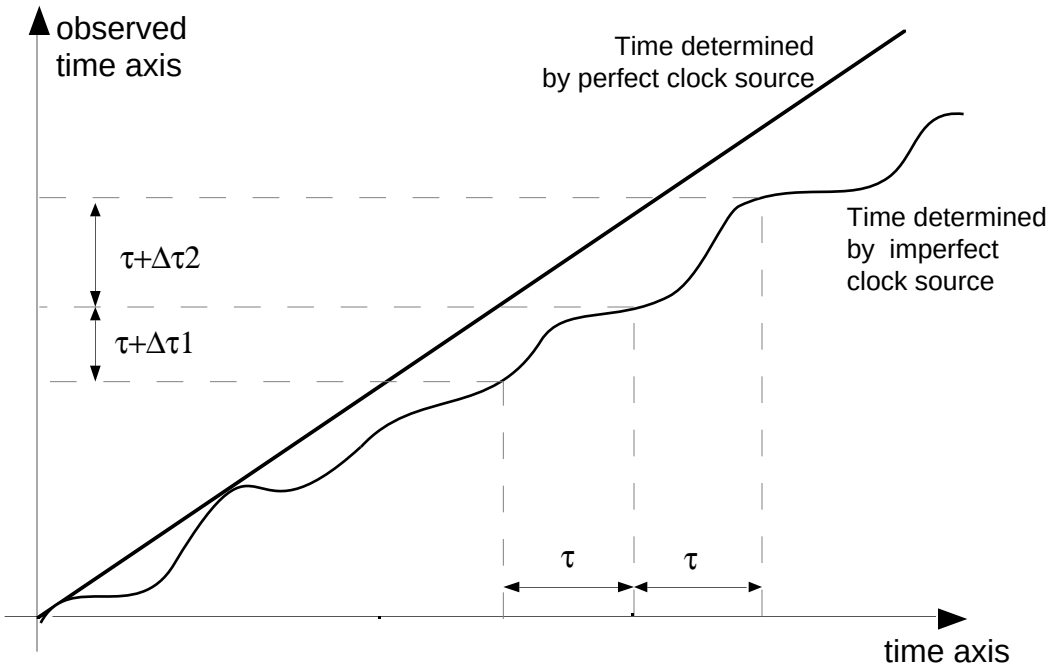


Figure 9: Definition of Time Interval Error

The observation time, τ, can be set to any convenient value (it is independent of clock frequency). At the end of the observation time interval a measure is made of how much the observed imperfect clock has deviated from the perfect clock (the phase difference). Longer observation times should produce larger values of $\Delta\tau$. The MTIE for a certain observation interval is simply the maximum TIE that results from an infinite number of TIE measurements, each performed after a certain observation interval. Practically, the number of measurements performed before MTIE is declared must be limited, perhaps to the total number of observation intervals that would fit into a couple of hours. Even so, a measure of MTIE for a number of different observation intervals would require a prohibitively long period of time. However, MTIE measurements can be performed in a more efficient manner. The maximum wander frequency by definition is 10 Hz so it is possible to completely describe the wander signal up to 10 Hz if the TIE is sampled at twice this rate (the Nyquist rate of 20 Hz – it is probably better to use a higher rate to avoid any aliasing). The TIE can be measured and recorded at 50 ms intervals, then by setting different "sliding windows" equal to different observation intervals, the maximum TIE values can be determined by grouping the measured values into the sliding windows. A constant frequency offset will produce the same MTIE value for a given observation period; MTIE will increase linearly with increasing observation time. MTIE is a good metric of frequency offsets between an observed clock and a perfect clock. It will also show a record of any phase transients (one-shot phase jumps). Increasing observation times will show an increasing MTIE until the maximum deviation is reached, at which point MTIE will stay at a constant value for larger values of observation time.

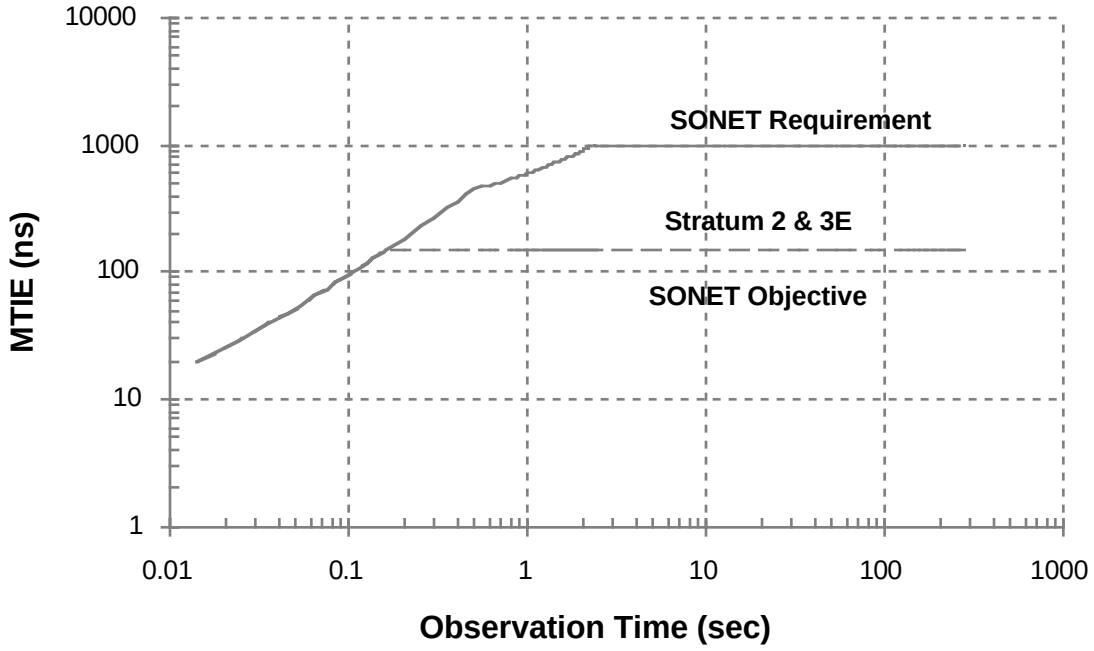


Figure 10: GR-253 MTIE limits on Frequency Offset/Phase Transient

MTIE does not reveal how “noisy” the observed clock signal is. The TDEV measurement is used to represent the spectral components of the observed clock. To measure TDEV the same TIE measurements previously collected at 50 ms or faster are used along with digital signal processing filtering to quantify the spectral components. The DSP filter (figure 11) blocks DC, therefore frequency offsets are not included in this measurement. Any phase transients that may happen do so rarely and any resulting energy from these transients will integrate out over the long integration intervals.

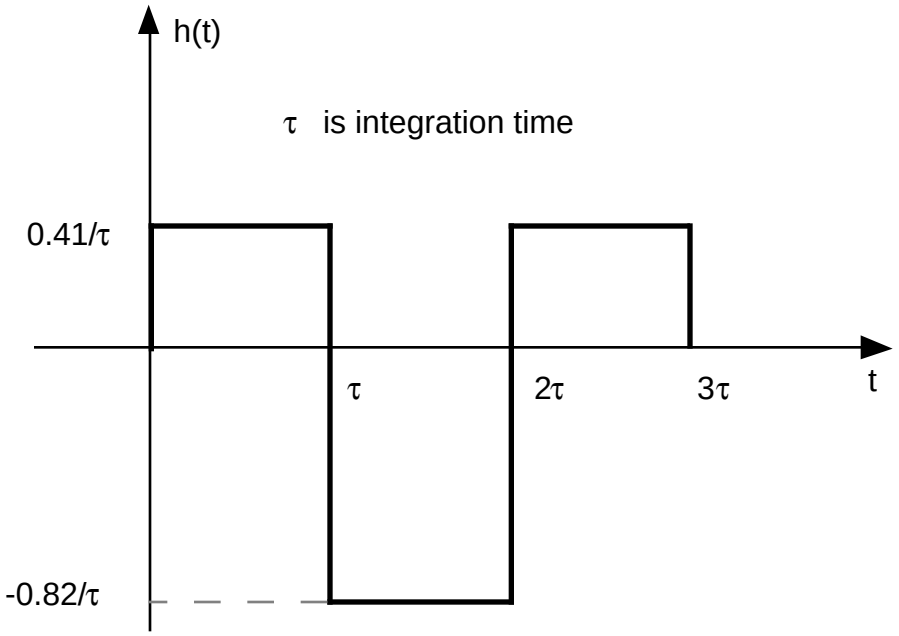


Figure 11: Impulse Response of DSP TDEV filter

Bellcore GR-253-CORE, December 1995; ANSI T1.101-1994 specifications:

Bellcore and ANSI have specified limits to wander at interfaces to SONET systems. The specifications cover five different areas of wander:

1. Short term stability. This is a measurement of the wander on the outgoing OC-N signal produced by the equipment when the input reference is wander-free.

2. Wander Transfer. This is a measurement of the amount of wander that is transferred from a “wandering” input reference to the outgoing OC-N signal. The input reference clock wander is modulated to meet a given mask (figure 12 below).

3. Phase Transient Criteria. When the equipment changes reference, the resulting phase transient will produce wander. No errors should result when switching reference or changing timing modes.

4. Derived DS1 Wander. The OC-N signal can be used to generate DS1 timing (e.g.., for BITS reference), and this process will produce wander even if the OC-N signal is wander-free[4].

5. Interface Wander. ANSI limits the amount of wander on both DS1 and OC-N signals at specific interface points.

Wander Transfer (Section 5.4.4.2.4, Req 5-126, 5-127, 5-128):

An externally-timed SONET NE must meet the TDEV curve when wander with magnitude equal to the MASK curve (figure 12, below) is input (note that an NE meeting this requirement will automatically meet the jitter transfer requirement).

A SONET NE's output OC-N or STS-N signal must meet the requirement curve below when referenced to an input OC-N or STS-N signal that meets the same curve.

In the pass band, the phase gain of the SMC shall be smaller than 0.2dB.

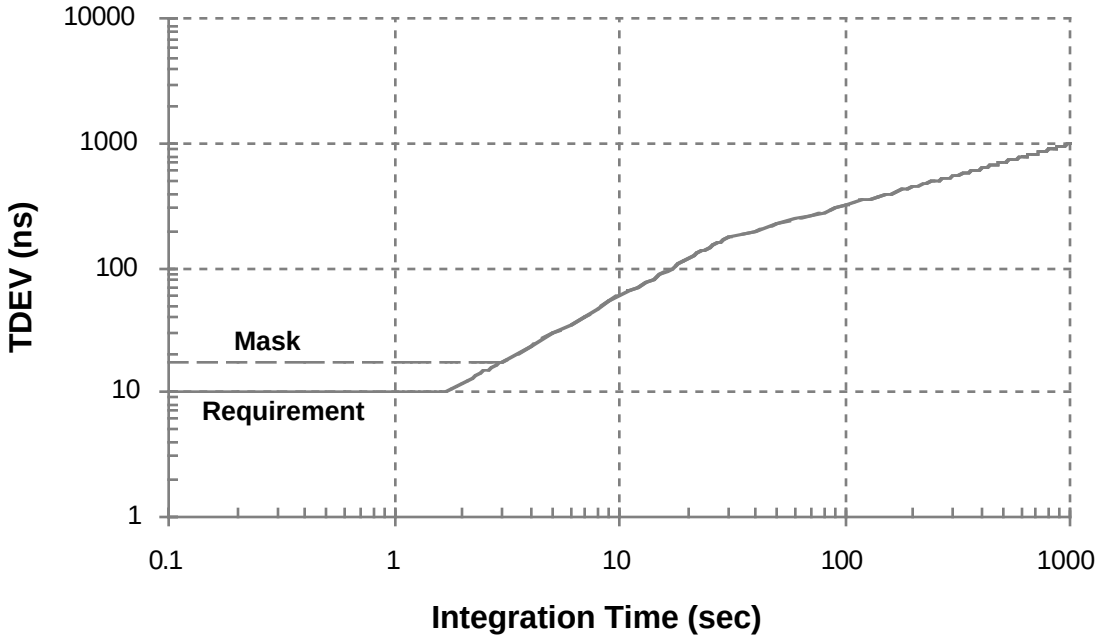


Figure 12: Wander Transfer Requirement

Wander Generation (Section 5.4.4.3.2, Req 5-130, 5-131):

A SONET NE optical or electrical output must meet the MTIE and TDEV wander curves of figure 13 and 14. Conformance to this requirement is tested with a wander-

[4] Flicker noise will induce phase fluctuations in a VCXO even with a fixed control voltage.

free reference having bandlimited white noise phase modulations (jitter) of 1000 ns p-p. The jitter is bandlimited with 3dB cut-off frequencies at 10 Hz and 150 Hz. This specification tests the short term stability of the clock source. Note that not all VCXO clock sources will be able to meet both wander generation and wander transfer requirements.

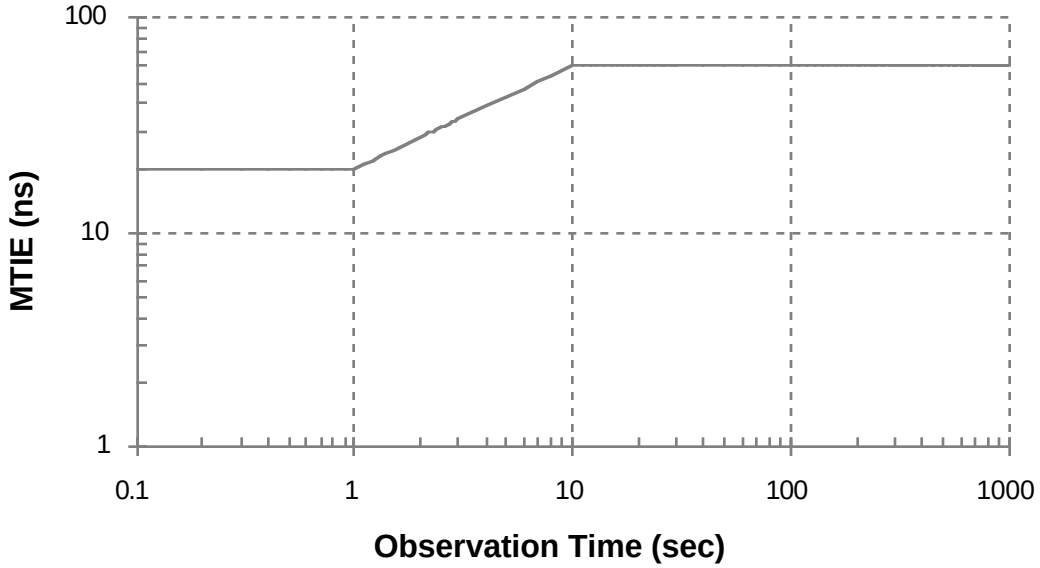


Figure 13: MTIE Wander Generation Requirement

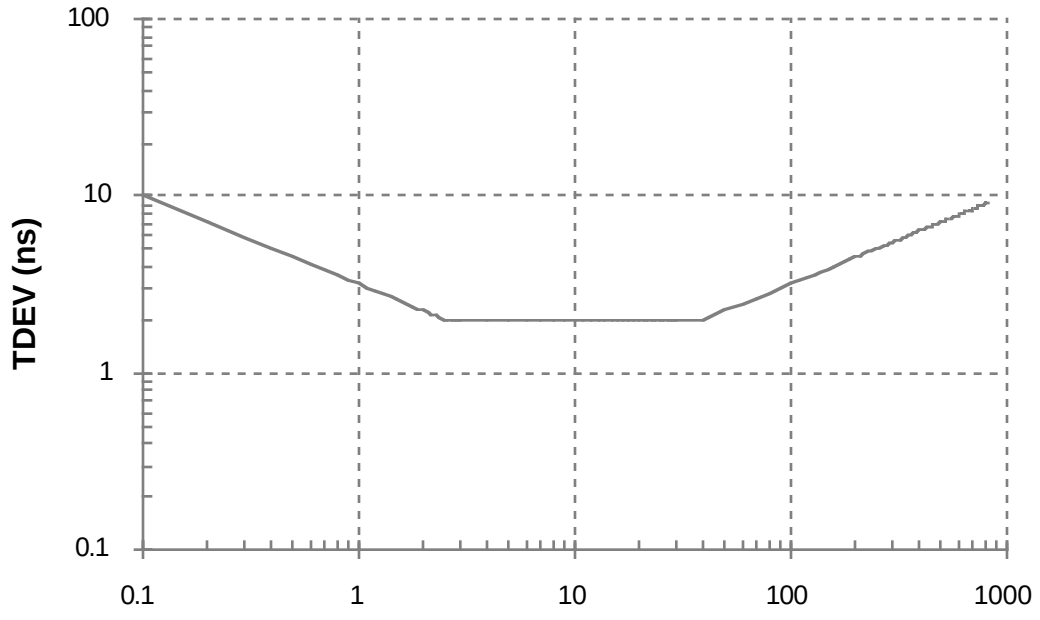


Figure 14: TDEV Wander Generation Requirement

Jitter:

Jitter related specifications for SONET/SDH equipment are given in GR-253-CORE, ANSI T1.105, ANSI T1.646 , ITU-T/CCITT G.825 & G.958. Jitter specifications for ATM equipment are given in the ATM Forum UNI 3.1 specification.

The jitter specifications defined in GR-253-CORE and ITU-T G.825 fall into several categories: interface jitter; jitter generation; jitter tolerance; and jitter transfer.

Interface jitter and jitter generation categories are measured in absolute values of jitter at designated interface points. These are WAN specifications and are required to be met by any equipment used in the WAN. Network planners rely on these values when projecting new routes or changes to existing ones. LAN equipment does not necessarily have to meet these two requirements, however, the ATM Forum UNI specification refers to the GR-253 specifications as a requirement.

Jitter tolerance and jitter transfer categories for WAN equipment are specified based on a hypothetical network model as defined in ITU-T G.801. G.801 specifies a standard digital hypothetical reference connection with a maximum length of 27500 km. These network models are hypothetical entities of defined length and equipment composition for use in studying the effects of digital transmission impairments such as bit errors, jitter and wander, transmission delay, and slips on the overall network performance. These specifications for jitter tolerance and jitter transfer are not absolute and, strictly speaking, are not necessary for equipment to operate correctly. It is a good practice, however, to comply with these specifications so that severe network impairments can be minimized. Again, for LAN applications, the network span is small so jitter tolerance and jitter transfer effects cannot accumulate; there should be no need to meet the WAN specifications for jitter tolerance and jitter transfer. However, the WAN jitter tolerance is useful for determining clock recovery jitter margin in the LAN.

Interface Jitter

Bellcore GR-253-CORE Dec.1995 and ANSI T1.105.03-1994: (Bellcore Section 5.6.1, Req 5-201; ANSI Section 5, Table 7)

Timing jitter at the network interface shall not exceed A1 Unit Intervals peak-to-peak (UIpp) when measured over a 60-second interval with a bandpass filter having a high-pass cutoff frequency of B1 and a low-pass cutoff frequency of at least B3; each filter has a roll-off of 20 dB/decade.

Timing jitter at the network interface shall not exceed A2 Unit Intervals peak-to-peak (UIpp) when measured over a 60-second interval with bandpass filter having a high-pass cutoff frequency of B2 and a low-pass cutoff frequency of at least B3; each filter has a roll-off of 20 dB/decade.

OC-N/STS-N level	B1 (Hz)	B2 (kHz)	B3 (MHz)	A1 (UIpp)	A2 (UIpp)
1	100	20	0.4	1.5	0.15
3	500	65	1.3	1.5	0.15
12	1000	250	5	1.5	0.15
48	5000	1000	20	1.5	0.15
48(B)	5000	12	20	1.5	0.15

Table 3: GR-253 Interface Jitter

ITU-T /CCITT G.825, March 1993 (Section 3.1, Table 1):

At any SDH network interface, the following jitter specifications must be met:

Timing jitter as measured over a 60-second interval with a bandpass filter with a lower cutoff frequency of f1 and a minimum upper cutoff frequency f4 shall not exceed B1 Unit Intervals (UI) peak-to-peak. Also, timing jitter as measured over a 60-second interval with bandpass filter with a lower cutoff frequency of f3 and a minimum upper cutoff frequency f4 shall not exceed B2 Unit Intervals (UI) peak-to-peak. The roll off at the lower cut-off frequency and upper cut-off frequency shall be 20dB/decade.

STM level	f1 (Hz)	f3 (kHz)	f4 (MHz)	B1 (UIpp)	B2 (UIpp)
STM-1	500	65	1.3	1.5	0.15
STM-4	1000	250	5	1.5	0.15
STM-16	5000	Under study	20	1.5	0.15

Table 4: G.825 Interface Jitter

This is the same specification as in GR-253-CORE.

ANSI T1.646 ," Broadband ISDN Physical Layer Specicifation for User-Network Interfaces, Including DS1/ATM , 1995(Section 7.6 .2..4):

This specification deals with the 155.52 Mbps Physical Layer Interface with LED into Multimode Fiber (MMF) . Here, the interface jitter is specified separately for the transmitter and the receiver in terms of contributions to “eye closure”.

Transmitter Characteristics:

The worst case interface jitter at the transmitter output shall be less than 1.6 ns for systematic jitter and 0.6ns for random jitter.

Rise and fall times of the transmitter should be less than 3.0ns. This specifies one of the bandlimiting factors of the system that influence the receive jitter tolerance. Overshoot is limited to 25 percent.

Receiver Characteristics:

The worst case interface jitter at the receiver input shall be less than 2.0 ns for systematic jitter and 0.6ns for random jitter.

The minimum receiver eye opening shall be 1.23 ns.

ATM Forum Technical Committee AF-PHY-0046.000, January 1996 (Section 2):

This specification deals with the 622.08 Mbps Physical Layer.

Single Mode Fiber:

The interface jitter is defined in ANSI T1.646, which points to T1.105.03 which is the same as GR-253-CORE.

Multi-Mode Fiber:

Again, jitter is defined in terms of contributions to eye closure.

Transmitter Characteristic:

The systematic interface jitter at the transmitter output shall be less than 0.40 ns peak-to-peak. (0.249 UI pp).

The random interface jitter at the transmitter output shall be less than 0.15 ns peak-to-peak. (0.093 UI pp).

Receiver Characteristic:

The systematic interface jitter at the receiver input shall be less than 0.50 ns peak-to-peak. (0.311 UI pp).

The random interface jitter at the receiver input shall be less than 0.15 ns peak-to-peak. (0.093 UI pp).

The minimum receiver eye opening at a 10^{-10} BER shall be 0.31ns.

Jitter Generation

Bellcore GR-253-CORE , December 1995 (Section 5.6.2.3.6, Req 5-221):

A jitter generation criteria exists for both Category I and Category II interfaces. Category I interfaces are defined as asynchronous DSn interfaces to a SONET NE; Category II interfaces are defined as OC-N, STS-N electrical and synchronous DS1 interfaces to a SONET NE (synchronous DS1 interfaces are DS1 interfaces where the incoming DS1 is byte-synchronously mapped into a VT SPE). For Category I interfaces the jitter generation criteria is divided into two areas: mapping jitter generation and pointer adjustment jitter generation. For both Category I and Category II, jitter generation is measured with no jitter or wander applied at the input. Furthermore, a bandpass filter is used to limit the jitter generation measurements. For OC-N and STS-N, the bandpass filter has a 12 kHz highpass cutoff frequency with a roll-off of 20 dB/decade and a lowpass cut-off frequency of at least B3 (from Table 3: GR-253 Interface Jitter).

The jitter generated at Category II interfaces shall be less than 0.01 UI rms, and shall also be less than 0.10 UI pp.

ITU-T G.958, November 1994 (Section 9.3.1):

An SDH regenerator shall not generate more than 0.01 UIrms jitter, with no jitter applied at the STM-N input. The measurement bandwidth and technique are under study.

ITU-T G.783, January 1994 (Section 6.1.2):

An SDH Add-Drop Multiplex and Cross-connect shall not generate more than 0.01 UIrms jitter as measured with 12 kHz high-pass.

Jitter Tolerance

Bellcore GR-253-CORE, December 1995 (Section 5.6.2.2.2, Req 5-209, Fig 5-28):

STS-N and OC-N interfaces, with the exception of OC-48 interfaces, shall tolerate, as a minimum, input jitter applied according to the mask in table 5 and figure 15, below.

OC-N	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (Hz)	f4 (Hz)	A1 (UIpp)	A2 (UIpp)	A3 (UIpp)
1	10	30	300	2k	20k	0.15	1.5	15
3	10	30	300	6.5k	65k	0.15	1.5	15
12	10	30	300	25k	250k	0.15	1.5	15

Table 5: GR-253 Input Jitter Tolerance

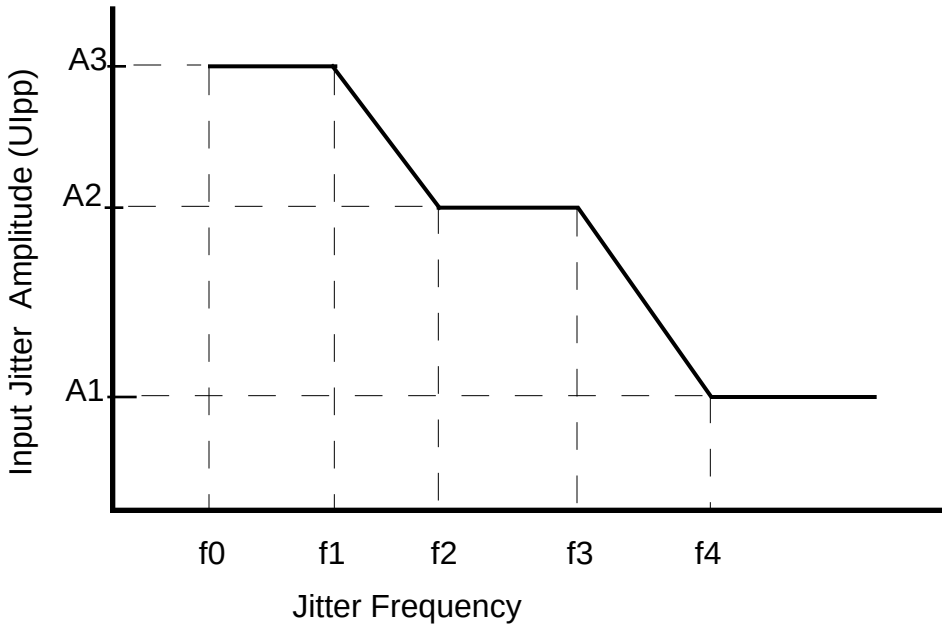


Figure 15: Input Jitter Mask

ITU-T G.958, November 1994 (Section 9.3.3):

Jitter tolerance in G.958 is defined the same as in GR-253-CORE. The one exception is the 15 UIpp amplitude at low frequency is not required. This specification is valid for ADM and Type A regenerators (i.e., those devices that meet the jitter transfer of Table 9) and is given in Table 6. Type B regenerators (i.e., those devices that meet the jitter transfer of Table 10) have reduced tolerance requirements (Table 7).

STM-N	f0 (Hz)	f1 (Hz)	A1 (UIpp)	A2 (UIpp)
1	6.5k	65k	0.15	1.5
4	25k	250k	0.15	1.5
16	100k	1M	0.15	1.5

Table 6: G.958 Jitter Tolerance (Type A)

STM-N	f0 (Hz)	f1 (Hz)	A1 (UIpp)	A2 (UIpp)
1	1.2k	12k	0.15	1.5
4	1.2k	12k	0.15	1.5
16	1.2k	12M	0.15	1.5

Table 7: G.958 Reduced Jitter Tolerance

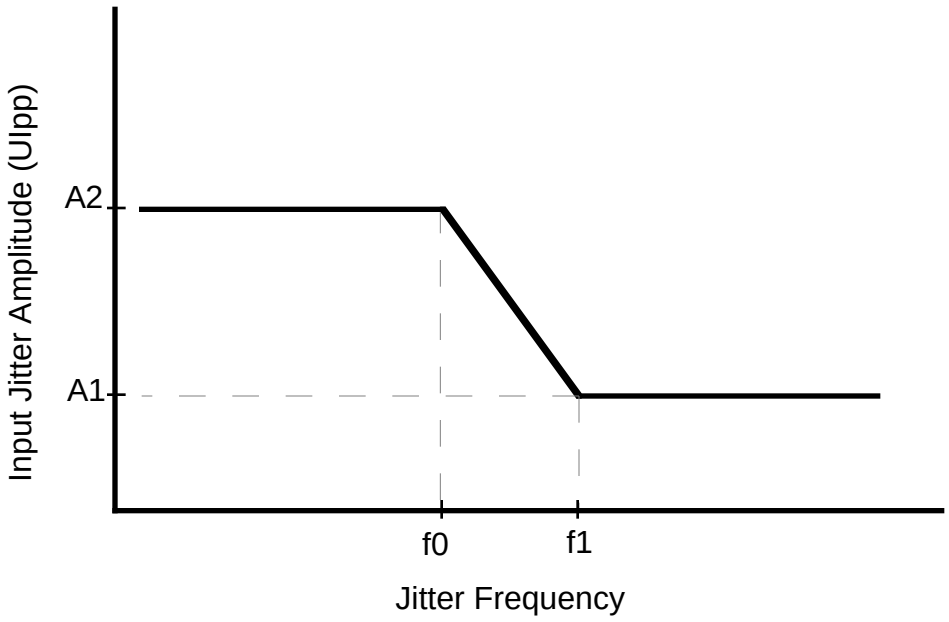


Figure 16: G.958 Input Jitter Tolerance

Jitter Transfer

Bellcore GR-253-CORE, December 1995 (Section 5.6.2.1.2, Req 5-205, Fig 5-27):

Jitter transfer for Category II interfaces shall be under the following mask (Table 8):

OC-N	f0 (Hz)	P (dB)
1	40k	0.1
3	130k	0.1
12	500k	0.1

Table 8: GR-253 Jitter Transfer

ITU-T G.958, November 1994 (Section 9.3.2):

Jitter transfer requirements for ADM and Type A regenerators (Table 9):

STM-N	f0 (Hz)	P (dB)
1	130k	0.1
4	500k	0.1
16	2000k	0.1

Table 9: G.958 Jitter Transfer (for Type A)

Jitter transfer requirements for type B regenerators (Table 10):

STM-N	f0 (Hz)	P (dB)
1	30k	0.1
4	30k	0.1
16	30k	0.1

Table 10: G.958 Jitter Transfer (for Type B)

History of Requirements

In North America, the GR-253 specification is constantly evolving. In the past (pre-1994), GR-253 required that all equipment in the WAN meet the specifications for interface jitter, jitter tolerance, intrinsic jitter, and jitter transfer, as well as clocking requirements such as short term stability, interface wander, wander transfer, and holdover. This was a tough specification that required expensive system clocking cards and synchronization.

In December 1994, GR-253 was revised to reduce the timing requirements on equipment that was interfaced to the WAN in *line-timed* mode. In this mode, the transmit timing was derived directly from the received line, so only jitter tolerance, intrinsic jitter and jitter transfer were needed. The requirements for wander and holdover were removed.

Then, in December 1995, GR-253 was again revised, this time to add another requirement for the line-timed mode. In reducing the number of requirements in the Dec. 1994 specification, a problem arose with equipment deriving their timing from the line: in the event the receive line signal is lost, where would the transmit timing come from? Most practical solutions had a back-up timing source, typically an SMC, which would be switched in when the receive signal was lost; however, the SMC and the line timing were not in phase. This caused a *phase transient* to occur in the transmit timing, usually an abrupt phase change which resulted in receiving equipment slipping a bit and going out of frame alignment. This caused network impairment and loss of revenue during the recovery time. Therefore, the Dec 1995 revision added a phase transient requirement dictating that a switch to a back-up transmit clock shall be “hit-less”, i.e., it will not cause a bit error at the receiving equipment.

There is usually a 2 year “grace period” from the time a standard is approved to the time that equipment manufacturers are expected to implement the new requirements. Therefore, for equipment being designed now, it is recommended that the requirements of GR-253 Dec. 1995 be met. In addition, there is ongoing discussion in the study groups to bring back the wander requirements to GR-253, so it is probably best that they be considered during the design as well.

EQUIPMENT CLASSIFICATIONS

Location in the Network

The classification of equipment basically arises from its location in the network. In the WAN, the traditional telco equipment, such as ADMs and DCS, make up the SONET/SDH ring network. Networking equipment may be connected at the periphery or incorporated into the WAN directly.

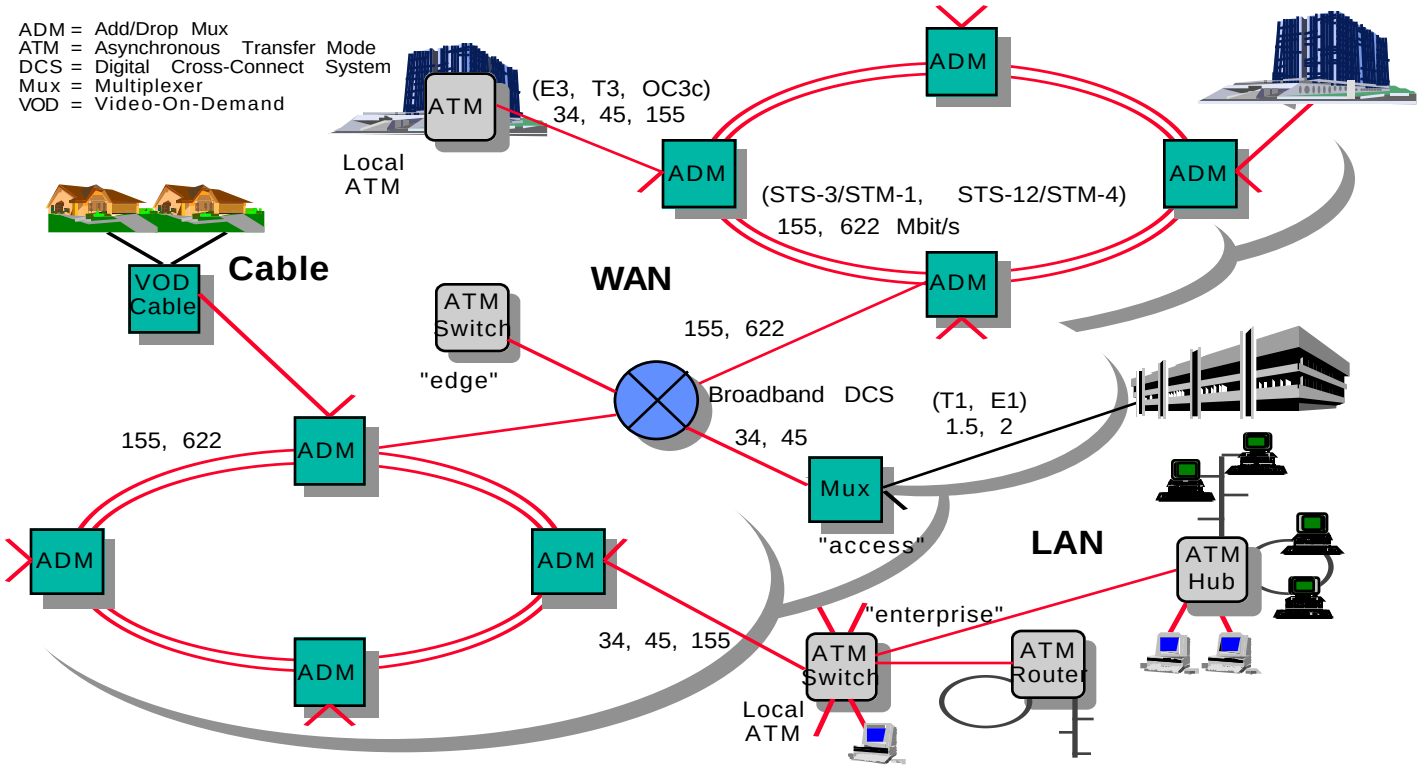


Figure 17: Typical WAN Network

Types of Equipment

Enterprise Switch

An Enterprise Switch is a premise-based system, privately owned and maintained which acts as the gateway interface between the local environment (LAN) and the public network (WAN). It acts as an aggregation point for WAN access, providing a wide range of both telephony and LAN interface options on the premise side, and providing WAN-compliant telephony interfaces (e.g. T1, T3, SONET) on the network

side. Enterprise switches are typically based on ATM technology and have a capacity of 5 GBits or more. They are used to interconnect campus switches, workgroup switches, routers, hubs, as well as integrate various disparate services (video, voice, ethernet, etc.) existing in the enterprise network. Both enterprise and campus switches can carry mission critical traffic. Various levels of hardware protection are an option.

Campus or Backbone Switch

This is a premise-based switch generally used to provide a local backbone for interconnecting various IP or ATM-based LAN equipment such as routers and workgroup switches. The Campus switch resides at the core of the private network. It may provide direct access to the WAN, or may access the WAN via an Enterprise switch.

Workgroup Switch

A Workgroup Switch resides in the LAN and provides desktop level switching services to ethernet client NICS. These switches are typically optimized for low-cost, high-performance workgroup applications, do not provide redundancy and are generally based on IP switching technology.

NIC

A Network Interface Card (NIC) resides within a desktop client computer, is generally based on ethernet technology (e.g. 10 Mbit/s or 100 Mbit/s) and provides client access to the LAN.

Core Switch

A Core Switch is a high capacity WAN switch used by public network service providers to provision their backbone network. Core switches typically provide only OC-3 rate interfaces or higher and have a capacity of 50 GB or more. Core switches generally interface directly only to other switching equipment in the public network such as Edge switches and Access muxes and not to customer equipment. As this class of switch is used in mission-critical public network applications, it will have a high degree of redundancy and fault tolerance.

Edge Switch

An Edge Switch is a high capacity WAN switch used by public network service providers to provision their backbone or access network. Edge switches typically provide only DS-3 rate interfaces or higher and have a capacity of 20 GB or more. Edge switches interface directly to both other switching equipment in the public network such as Core switches and Access muxes and to customer premise equipment such as Enterprise switches. Edge switches provide access services such as Frame Relay and ATM to end customers, provide aggregation of customer traffic

and provide high speed trunk interfaces to the public backbone network. As this class of switch is used in mission-critical public network applications, it will have a high degree of redundancy and fault tolerance.

Access MUX

An Access MUX provides traffic aggregation of a number low speed interfaces to a single high speed trunk interface. Access muxes are used in both public and private networks, and are based on either TDM or ATM technology. In a private network, the Access Mux provides a gateway to the WAN (similar to an Enterprise switch), aggregating traffic from a range of local equipment including PBX's, video conference systems, routers, and backbone switches. In a public network, the access mux is used to provide WAN access services to private networks (e.g. T1 Frame Relay or T1 ATM) and aggregating this traffic onto a single higher speed link to an Edge or Core switch. In mission-critical public network applications, Access MUXes will have a high degree of redundancy and fault tolerance.

APPLICABLE STANDARDS REQUIREMENTS

What really needs to be met

The equipment classification really boils down to two distinct types: “mission-critical” equipment, and “other”. Mission-critical equipment is that which cannot tolerate outages (Core switches, Edge switches, Access Mux,Enterprise ,Backbone equipment); it must have a high availability/reliability because a lot of traffic may be going through it or it is interfacing to public network equipment which, in turn, cannot tolerate outages. “Other” equipment is that which resides in the LAN or customer premise (Enterprise, Campus, Workgroup, NIC). Here redundancy is rarely provided as outages are more tolerable; these outages typically do not affect a large number of users and the services provided typically do not generate revenue.

The requirements on mission-critical equipment can further be classified by the timing mode the equipment is configured for.

External Timing Mode:

Equipment that has an available BITS clock must use external-timing. This equipment has to provide wander filtering to meet the wander requirements, including wander transfer, therefore it will automatically meet the jitter transfer requirement. Jitter generation and jitter tolerance requirements must also be met.

Holdover is also required for this external-timing mode. The overall stability during a 24 hour period and with temperature changes must be less that ±4.6 ppm (Stratum 3 clock).

Phase transient criteria also has to be met. During synchronization rearrangement the operating MTIE should be no greater than the requirement mask in figure 10. Rearrangement can occur due to:

1) Manual timing reference switching
2) Automatic timing reference switching due to LOS, AIS, LOF or Synchronization Status Message changes.
3) Entry into self-timing operation (holdover or free-run).
4) Phase transients of an external or OC-N synchronization input with specified rate of change.
5) Clock hardware protection switching.

Line Timing Mode:

Equipment that does not have an available BITS clock can use line-timing. Equipment in this timing mode must meet wander transfer and wander generation specifications. Since the line timing this equipment is referenced to already meets the wander transfer TDEV specification, then this equipment is not required to filter wander. The

transmit clock PLL bandwidth can therefore be as wide as the jitter transfer specification will allow. The wander generation specification can still be met with this wide bandwidth.

The specification for phase transients and holdover are same as for externally-timed equipment. These can only be met with a narrow transmit clock PLL bandwidth, somewhere in the order of 10-20 Hz. This narrow loop bandwidth will automatically meet the jitter transfer requirements. Jitter generation and jitter tolerance requirements will still need to be met.

Loop Timing Mode:

Some equipment may simply be loop-timed. The requirements for loop-timing are not as strict as those for line-timing:

1) the phase transient criteria is looser: it is an objective to meet the Requirement curve of figure 10. To meet this requires a narrow transmit clock PLL bandwidth, thereby automatically meeting the jitter transfer requirement;

2) holdover is not currently a requirement (this may change in the future);

3) clock accuracy has to be ±20 ppm and must meet the SMC requirement for a SONET minimum clock. This implies that the clock be more than just a 20 ppm fixed oscillator;

4) interface jitter, jitter tolerance, and jitter generation requirements still need to be met.

What does current equipment meet?

Most equipment is located in the LAN or interfaces into the WAN through an ADM or Access Mux. In most cases, this equipment is loop-timed and all that is necessary is to meet the interface jitter, jitter tolerance, jitter generation, and jitter transfer. Pragmatically, it is questionable whether the jitter transfer requirement really needs to met. Jitter transfer is a requirement of repeaters to limit the jitter gain; the interface equipment is typically connected directly to the WAN and does not go through any repeaters. As long as the jitter transfer curve of the equipment is flat (with peaking <0.1dB in the pass band) and eventually rolls-off (at a finite frequency somewhere between 130kHz and 500kHz), jitter gain is not a problem. The output from the WAN equipment meets the interface jitter requirements, and the input of the WAN equipment meets the jitter tolerance requirements; therefore, as long as the other, loop-timed equipment does not add jitter, the location of the transfer curve corner is irrelevant.

Going forward, the evolving GR-253 standard is placing more emphasis on the phase transient requirement, even for loop-timed equipment. This requirement adds complexity to the timing generation by requiring that the equipment fall back to an

SMC in the event that the received timing signal is lost. The fall-back must be such that the transmit signal is not disturbed. The practical benefit of this is that the transmitted data stream is unaffected by the receive stream.

Ultimately, the equipment requirements are subject to final “approval” by the intended recipient of the interface signal. For example, certain public network service providers may either waive specific requirements as unnecessary or may have their own, more stringent set of requirements for accessing their network. Unfortunately, in some cases meeting the WAN standards may be a necessary *but* not sufficient condition for equipment acceptance by the end customer.

What is met by PMC-Sierra Devices:

PMC-Sierra physical layer interface devices deal with most of the jitter requirements directly. The LAN PHY devices have been optimized for jitter tolerance, therefore, they will not meet the jitter transfer requirement with respect to the 130kHz corner frequency. Their typical transfer characteristic is flat (<0.1dB) up to the cut-off frequency of around 400kHz. As mentioned above, this is will not cause any operational issues.

The WAN PHY device has been optimized for both the jitter tolerance and jitter transfer requirements.

In all cases, these devices do not address the wander requirements; these can only be satisfied with external, narrow bandwidth clock circuits.

		Jitter			
Device	**Wander**	Tolerance	Generation	Transfer	**SSM**
PM5346 (LITE)	no	yes	yes	no	No (defaults S1 to 0000, STU)
PM5347 (PLUS)	no	yes	yes	yes	Yes
PM5348 (DUAL)	no	yes	yes	no	Yes

A CIRCUIT TO MEET THE WAN REQUIREMENTS

The following circuit provides a method of meeting the requirements of external-timed equipment using the S/UNI-PLUS[5]. Certain portions may be omitted if the equipment is to operate in line-timed or loop-timed, as the requirements are less onerous. However, even in the case of loop-timed, this circuit will still be necessary to achieve the phase transient requirement and the SMC requirement. If even these two requirements are not necessary, then the S/UNI-PLUS can be used on its own. If the equipment is being designed with devices whose performance has been optimized for jitter tolerance (such as the S/UNI-LITE or S/UNI-DUAL), then this minimum circuit is necessary to meet the jitter transfer requirement (a by-product of the narrow bandwidth PLL used to meet the phase transient requirement).

The timing circuit is a microprocessor-controlled VCXO. The PLL loop filter is implemented digitally within the microprocessor. An added benefit of using the micro is that accurate clock holdover can be achieved, and temperature compensation can be performed in software.

The block diagram (figure 18) below represents a single timing circuit. If hardware protection (i.e., redundancy) is required, two circuits would be used in a master-slave configuration to provide back-up timing that could be switched in the event of a timing failure.

The main component of the synchronization circuit is the phase locked loop. The PLL consists of a VCXO, a phase detector, digital loop filter (implemented in software in the microprocessor), and some selection circuitry (muxes) for choosing the reference signal and the appropriate comparison signal. In addition to implementing the loop filter, the microprocessor monitors the reference signal (for protection switching) and provides holdover and temperature compensation.

The VCXO has ±20 ppm frequency accuracy and a ±60 ppm frequency adjustment range. This wide adjustment range is necessary to satisfy the requirements for a SMC; the pull-in range for the SMC requires that the VCXO have a minimum frequency adjustment range of ±40 ppm, the ±60 ppm range provides some margin. The choice of VCXO is critical. The TDEV of the VCXO must be measured on its own (outside of the loop) to find its spectral performance. As well, the MTIE for the oscillator when free-running must be less than the 20 ns requirement for observation times below 1 second. These measurements check that the VCXO on its own can meet the wander generation requirements for integration and observation times shorter than 1 second.

[5] This circuit can also be used with the LAN PHY devices.

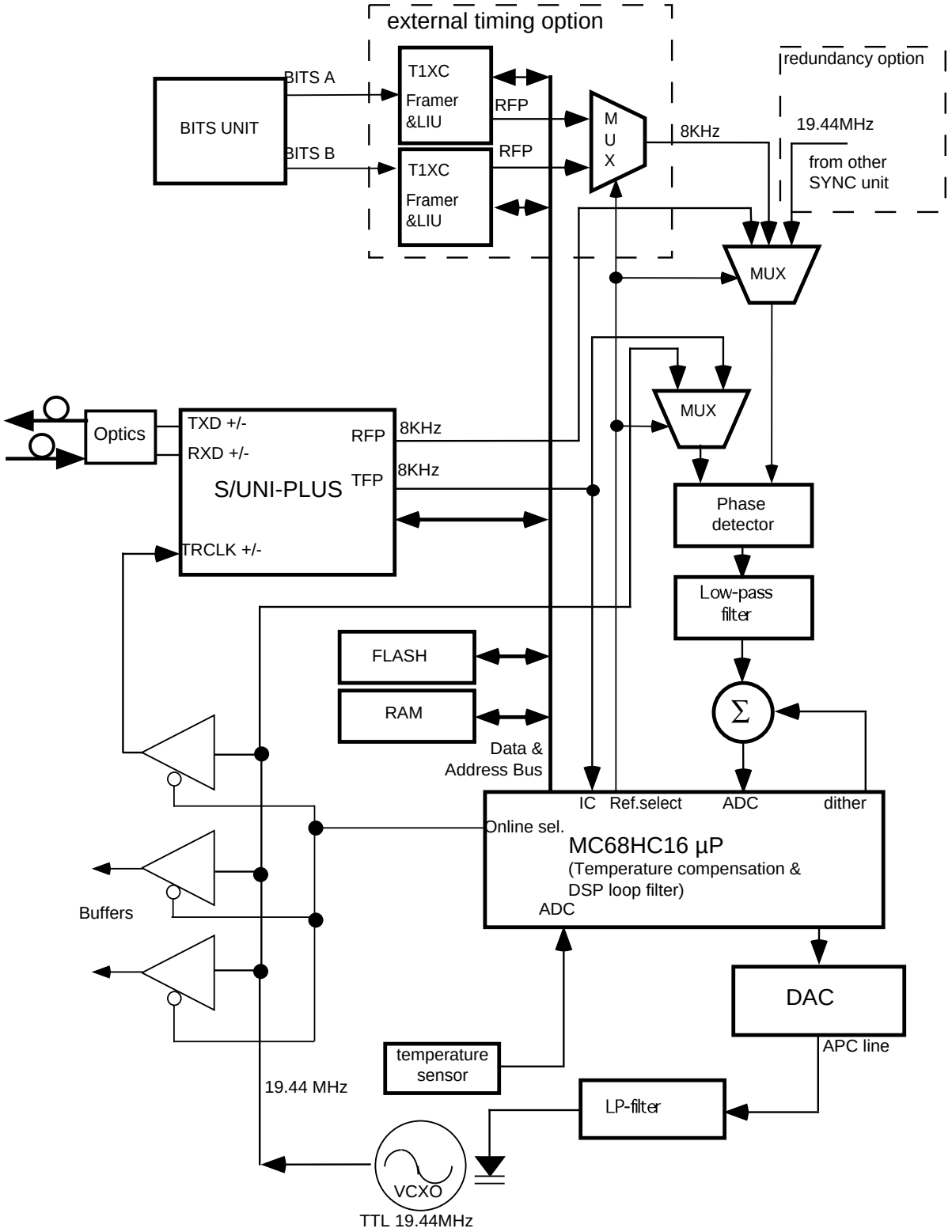


Figure 18: Microprocessor Controlled PLL

The reference clock for the PLL can be from many different sources, depending on the timing option used and whether redundancy is used. In the case of Line-timing or loop-timing, the PLL reference is the 8 kHz RFP (Receive Frame Pulse) signal from S/UNI-PLUS. In the case of external-timing with an available BITS source, the PLL reference is one of the two 8 kHz RFPO signals from T1XC devices that can receive the BITS clock. In the case of redundant timing, the PLL reference is the 19.44 MHz clock from the master clock circuit.

The feedback comparison signal for the PLL can be either the 8 kHz TFP (Transmit Frame Pulse) signal from the S/UNI-PLUS, or the 19.44 MHz transmit clock in the redundancy case where this circuit is the slave clock unit. The normal operating circuit (i.e., the master clock unit in the redundant case) will be using 8 kHz signals as the reference and comparison signals, while the slave clock circuit will use two 19.44 MHz signals to lock the VCXO. The difference in the loop gain due to the division by 2430 (in the normal operating case) is accounted for by the microprocessor.

The phase detector is simply two D-FFs with asynchronous resets (figure 19). The reference signal clocks one D-FF and the comparison signal clocks the other D-FF. The data inputs to both D-FFs is tied to logical one; the D-FF output will be set high each time the clock rising edge is sensed. The D-FF outputs are NANDed and the resulting signal is used to reset both D-FFs. Differences in propagation times between the two D-FF and their async reset times will cause a static phase offset between the VCXO output and reference. This will not distort the phase detector transfer function around the zero phase error “lock” point, but it will slightly decrease the phase error range from $\pm 2\pi$ at the -2π and $+2\pi$ limits. Processing the phase detector output within the microprocessor allows the detector transfer characteristic to be widened.

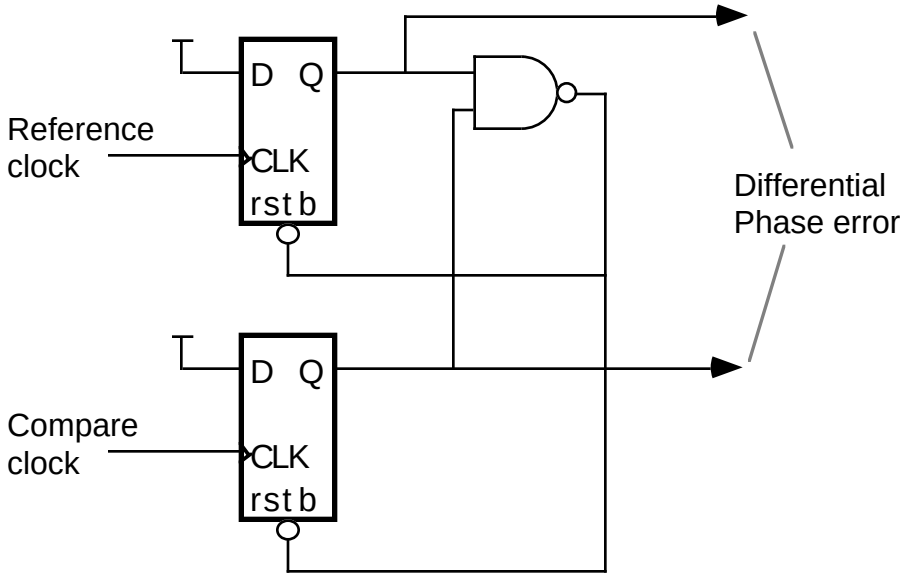


Figure 19: Phase Detector

A differential low-pass filter is used to filter the phase error signal before it is sampled by the ADC internal to microprocessor. This filter removes the high frequency (jitter) components that can alias through the digital filter and influence both MTIE and TDEV performance. The filter cut-off frequency (approximately 10 Hz) can attenuate the 8 kHz phase error signal by over 58 dB. At the same time this cut-off frequency is more than an order of magnitude higher than the dominant pole introduced by the DSP so any extra phase shift at frequencies below 1 Hz due to this anti-aliasing filter will be less than 5 degrees. At frequency of 0.3 Hz, the extra phase shift is less than 2 degrees.

The MC68HC16 microprocessor internal ADC is 10 bits, so it can resolve voltage changes down to approximately 5 mV. Phase error voltages below this value cannot be sensed with this ADC hence there will be small frequency offsets between the reference and the feedback signals that will not be detected for long periods of time. Only after these offsets accumulate and exceed the 5 mV threshold will the PLL be able to react. The result will be that low frequency wander will be introduced in the output even if there is no wander in the reference frequency. Dithering at a high frequency is used to improve the performance of the ADC. The dither signal frequency can be chosen to be one half of the sampling frequency of ADC and the dither amplitude can be on the order of the LSB. Averaging within the microprocessor will produce a signal with better resolution than the ADC alone (as well, 32-bit operations are used for digital filtering so that roundoff errors are small). The dither signal is supplied by the microprocessor itself. The input capture function of the microprocessor is used to run an interrupt service routine that performs the ADC and a “count-to-two”. The result of this count to two is summed via a resistor network with the output of the anti-aliasing filter to give the total signal that is converted by the ADC.

As mentioned, the input capture function is used to drive the ADC sampling rate. The TFP output of the S/UNI-PLUS is connected to the input capture (IC) pin of the microprocessor, thereby creating an 8 kHz ADC sampling rate. On every rising edge on IC, the DSP filtering of phase error signal is performed and the resulting value is output to a 12-bit DAC through the SPI port . The 12-bit DAC does not have enough resolution to satisfy the TDEV requirements of GR-253-CORE on its own, but a simple NCO with an MSB output can be used to dither the LSB of the DAC and improve the resolution. The dither frequency produced by a five bit binary (32 bit long periodic sequence, frequency= 8 kHz/32=250Hz) can be effectively removed by a low pass filter on the DAC output with a cut-off frequency of 25 Hz. This technique results in an equivalent performance of a 17-bit DAC which, using a 120 ppm VCXO, equates to 1 milli-ppm accuracy. The resulting MTIE and TDEV measurements are well below GR-253-CORE specification for wander generation.

The microprocessor, in addition to performing the digital filtering, also monitors and generates the Synchronization Status Messages in the S/UNI-PLUS. If external-timing is used, the microprocessor also monitors the SSM from the BITS sources. Furthermore, the microprocessor can monitor the performance of the optical link (LOS, AIS, LOF, BIP-8 from the S/UNI-PLUS) for an indication of the quality of the

OC-3 signal being used to line or loop-time to. Finally, if clocking redundancy is used, the microprocessor can monitor the status of the other timing circuit to determine when to switch to back-up.

The program code that runs the microprocessor is held in Flash PROM. In addition, the Flash PROM can be used to store temperature compensation information. There are a couple of ways to implement temperature compensation. The simplest way is to store the average values of frequency offsets vs. temperature for the VCXO (this information should be available from the manufacturer); this method should be able to achieve ±4.6 ppm in 24 hours over the given temperature change. The other method is more precise , but it involves recording in Flash the particular frequency offsets from nominal vs. temperature for the particular VCXO during temperature cycling. This method is capable of achieving less than ±1 ppm over a period of months, but it can be more expensive to implement because every timing circuit must be temperature cycled at a decreased rate (less than 1 °F per 2 minutes to avoid recording biased values due to inertia of the thermal process) in order to calibrate the VCXO. An added benefit of this method is that the on-board temperature sensor accuracy and DAC temperature dependency are calibrated as well.

Finally, it should be noted that in the case of external-timing with BITS clocks, the RFPO signal from the T1XC will contain up to 1/8 UIpp of jitter from the recovered PCM clock generated by the clock recovery block. This jitter is produced by the limited resolution of the digital PLL implemented in the receive clock recovery circuit of the T1XC. This jitter is high frequency and will be averaged out within the microprocessor.

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APPENDIX A

Derivation of Wander Contribution from Temperature Variations

Length of the fiber in open air: $L = 250{,}000$ m

Permittivity of free space: $\varepsilon_0 = 8.854 \bullet 10^{-12} \frac{farad}{m}$

Permeability of free space: $\mu_0 = 4 \bullet \pi \bullet 10^{-7} \frac{henry}{m}$

Velocity of light: $c = \frac{1}{\sqrt{\varepsilon_0 \bullet \mu_0}}$ $c = 2.99796 \bullet 10^{8} \frac{m}{sec}$

Index of refraction of pure silica fiber: $n = 1.46$

Propagation delay through fiber of length, L: $\tau = \frac{L \bullet n}{c}$ $\tau = 0.0012175$ sec

Temperature change in degrees Kelvin: $\Delta T = 1\ ^\circ K$

Temperature sensitivity of thermal expansion coefficient of silica: $\Delta L = 5 \bullet 10^{-7} \bullet \Delta T \frac{m}{^\circ K}$

Temperature sensitivity of refractive index: $\Delta n = -10^{-5} \bullet \Delta T \frac{1}{^\circ K}$

Change of propagation delay due to the temperature change:

$$\Delta\tau = \left(\frac{n}{c} \bullet \frac{\Delta L}{\Delta T} + \frac{L}{c} \bullet \frac{\Delta n}{\Delta T}\right) \bullet \Delta T$$

$\frac{L}{c} \bullet \frac{\Delta n}{\Delta T} = -8.339013934 \bullet 10^{-9} \frac{sec}{^\circ K}$ $\frac{n}{c} \bullet \frac{\Delta L}{\Delta T} = 2.434992069 * 10^{-15} \frac{sec}{^\circ K}$

$\frac{\Delta\tau}{\Delta T} = -8.3390115 \bullet 10^{-9} \frac{sec}{^\circ K}$

The fiber expansion term (ΔL component) is negligible, most of the change in delay comes from the change in the index of refraction. A 250km fiber line in open air gives -8.3ns/°K of delay; for OC-3, this is equivalent to:

$N = \frac{\Delta\tau}{\Delta T} \bullet 155.52 \bullet 10^{-6} \frac{UI}{sec}$ $\Rightarrow$ $N = -1.2969 \frac{UI}{^\circ K}$ $\Rightarrow$ $N \bullet 20^\circ K = -25.94$ UI

With a change of temperature of 1°K, the 250km length of fiber will produce approximately 1.3 bits difference between transmitted and received data rate. If the temperature change is 20 degrees (possible over a 24 hour period), it will result in approximately 26 bits difference! For fiber in ground, the ΔT is in the order of 2-3°K, which is still 2.6 to 3.9 bits difference.

Change in LASER wavelength due to change in temperature: $\Delta\lambda = 0.1 \bullet 10^{-9} \bullet \Delta T \frac{m}{°K}$

Change in index of refraction as a function of wavelength change:

$\Delta n_{1300} = 3 \bullet 10^{5} \bullet \Delta\lambda \frac{1}{m}$ at 1300 nm, there is little change because of negligible chromatic dispersion

$\Delta n_{1500} = 51 \bullet 10^{5} \bullet \Delta\lambda \frac{1}{m}$ at 1500 nm, index of refraction changes due to the change of wavelength

LASER temperature change results in wavelength change that results in delay difference:

$$\frac{\Delta\tau}{\Delta T} = \frac{L}{c} \bullet \frac{\Delta n}{\Delta\lambda} \bullet \frac{\Delta\lambda}{\Delta T} \frac{UI}{sec} \quad \Rightarrow \quad \frac{\Delta\tau}{\Delta T} = 4.2529 \bullet 10^{-7} \frac{sec}{°K}$$

NOTES

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